一款 VDMOS 半超结元胞结构的设计

刘 铭，冯全源，庄圣贤
（西南交通大学 微电子研究所，四川 成都 611756）

摘 要： 设计了一款 VDMOS 器件的元胞结构，采用半超结结构模型. 传统 VDMOS 结构的导通电阻会随着击穿电压的增长而增长，而半超结结构可以缓和两者之间的矛盾. 通过调节工艺条件，经过三次外延注入生长形成 P 柱，并采用增大外延层浓度和改善电荷平衡的方式，来达到减小元胞结构的特征导通电阻和提高击穿电压的目的. 最终实现了 1 005 V 的耐压，特征导通电阻 102.91 m$\Omega * cm^2$，栅漏电容 5.65 pF/cm^2，阈值电压 3.45 V 的元胞结构，降低了超结结构的工艺难度，并获得较优的性能.

关键词： 特征导通电阻；栅漏电容；击穿电压；半超结

中图分类号： TN386 **文献标识码：** A **文章编号：** 1000－7180(2015)12－0049－05

Design of VDMOS Semi-super Junction Cell Structure

LIU Ming, FENG Quan-yuan, ZHUANG Sheng-xian
(Institute of Microelectronics, Southwest Jiaotong University, Chengdu 611756, China)

Abstract: The cell structure of VDMOS has been designed by Semi-super junction. The specific On-resistance in traditional VDMOS structure will increase as the growth of the breakdown voltage. While the Semi-super junction can ease the contradictions between Specific On-resistance and breakdown voltage. By the regulation of the process flow, P column has been achieved in the three times epitaxial growth. In order to reduce specific on-resistance and keep the high voltage, the epitaxial concentration has been increased and charge balance of the cell structure has been formed. The breakdown voltage 1005 V and the specific on-resistance 102.91 m$\Omega * cm^2$ have been achieved with the cell structure. The gate-drain capacitance was 5.65pf/cm^2 and the threshold voltage was 3.45 V. Compared with the super junction, Semi-super junction was reduced the process difficulty. What's more, Semi-super junction devices have excellent performance.

Key words: specific on-resistance; gate-drain capacitance; breakdown voltage; semi-super junction

作者简介：
刘 铭 男，(1990-)，硕士研究生. 研究方向为大功率器件的研究与设计.
冯全源（通讯作者） 男，(1963-)，博士，教授，博士生导师. 研究方向为数字、模拟及射频集成电路设计. E-mail: fengquanguan@163.com.
庄圣贤 男，(1964-)，教授，博士生导师. 研究方向为 SoC 系统设计方法、电力电子系统控制与集成.

收稿日期： 2015－03－17；**修回日期：** 2015－04－30
基金项目： 国家自然科学基金项目(61271090)；四川省科技支撑计划项目(2015GZ0103)