高速串行接口接收端阻抗校正电路设计

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摘 要：研究并设计了一款应用于高速串行接口接收端的阻抗自校正电路，用以降低因接收器输入端阻抗不匹配而造成的信号反射，提高信号完整性. 阻抗自校正电路采用由比较器和阻抗校正单元组成的数模混合负反馈环路结构，其中阻抗校正单元由有限状态机和接收端电阻阵列的复制单元构成，且电阻阵列由46个相同的电阻单元和一个半权重电阻单元并联组成. 仿真验证显示，阻抗自校正电路实现了3%的校正精度，±35%的校正范围，回波损耗(S_{11})在12.5 GHz时小于−15 dB. 该电路在55 nm CMOS工艺设计，面积为218 μm×133 μm，功耗为7.43 mW.

关键词：高速串行接口；阻抗自校正；数模混合；校正精度；回波损耗
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An Impedance Calibration Circuit Design of High-speed Serial Interface Receiver

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Abstract: An impedance self-calibration circuit applying to high-speed serial interface receiver was studied and designed. It is used to reduce the signal reflection because of impedance mismatch of the receiver input channel and improve the signal integrity. Impedance self-calibration circuit using digital-analog hybrid negative feedback loop structure which is composed of comparator and impedance calibration unit. The impedance calibration unit is made up of finite-state machine and replication cell of the receiver resistor array, and the resistor array consist of 46 same resistor unit and one half-weight resistor unit with parallel hybrid. Simulation and verification indicates that the calibration precision of the impedance self-calibration circuit can reach to 3% and calibration range can reach to ±35%, when the frequency is 12.5 GHz the return loss is less than -15 dB. The chip was taped out in 55 nm CMOS technology, it occupied 218 μm×133 μm and the power consumption is 7.43 mW.

Key words: high-speed serial interface; impedance self-calibration; digital-analog hybrid; calibration precision; return loss

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