应用于全数字锁相环的高性能数控振荡器设计

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摘 要：全数字锁相环(ADPLL)是现代通信系统和计算机接口电路中的关键部件.数控振荡器(DCO)是ADPLL的核心模块电路，决定了ADPLL的整体性能.对比提出了一种基于标准单元技术的数控振荡器，采用粗调级与精调级级联的结构.该结构中的阶梯型粗调级，能够展宽频率调节范围、降低功耗；精调级采用插值电路，能够将粗调单元的延时步长细化，从而得到更高精度的输出时钟.基于Tower Jazz 0.18 μm CMOS工艺，对该数控振荡器进行了仿真验证，显示该电路能够工作在不同的工艺角、温度下，输出200 MHz的时钟信号，频率分辨率为10 ps，功耗为1.2 mW，而且线性度高.该数控振荡器完全基于标准单元设计，通过数字流程实现，具有更高的可移植性，缩短了设计周期.

关键词：全数字锁相环，数控振荡器，级联结构，阶梯型粗调级，插值电路
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Design of High Performance Digitally Controlled Oscillator for All-Digital Phase-Locked-Loop Application

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Abstract: ADPLL is the key component of modern communication system and computer interface circuits, and is applied in a large variety of situations. DCO is the most fundamental module in ADPLL, and influences the overall performance of it. A standard cell based DCO is proposed in this paper, in which the cascaded structure is used. The ladder shaped coarse-tuning stage can widen the operating range and save power consumption. Interpolation Circuits are adopted in the fine-tuning stage, and further improve frequency resolution to achieve a more accurate output clock. Simulation and verification are done about the DCO based on Tower Jazz 0.18um CMOS process. The results show that the DCO can operate under different corners and temperature, output clock signal of 200MHz with the frequency resolution of 10ps, and consume power up to 1.2 mw with high linearity and monotony. Moreover, the DCO can be totally designed by standard cells and implemented by digital flow, so has more portability and shorter turn-around time.

Key words: ADPLL; DCO; cascaded structure; ladder-shaped coarse-tuning stage; interpolation circuits

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