

SpaceWire 总线的流量控制机制研究

赵云富, 吴一帆, 孙 强, 许 娜, 吴 军

(北京控制工程研究所, 北京 100190)

摘 要: 为了解决 SpaceWire 总线在进行大数据块收发时, 现有的流量控制措施会导致总线性能下降的问题, 提出了一种两级存储结构, 介绍了 SpaceWire 总线目前的应用状况, 以及存在的问题; 通过分析 SpaceWire 的流量控制机制以及影响总线效率、系统性能的因素, 提出了一种能够保证第一级存储器有足够的空间用于收发数据的两级存储结构; 根据 SpaceWire 总线协议和两级存储结构, 设计了一款通过硬件预取技术实现大数据块传输的 SpaceWire 节点 IP 核; 最后在 Leon3-FT 处理器上集成了该 IP 核, 并进行了系统级的仿真和测试, 结果表明, 与现有的 SpaceWire 接口相比, 本设计在大数据块传输中能够提高总线效率 62.7 倍, 系统处理效率提高至少 14.5 倍。

关键词: SpaceWire 总线; 流量控制机制; 大数据块; 两级存储器; 硬件预取

中图分类号: TP393.03

文献标识码: A

文章编号: 1000-7180(2016)01-0001-05

Research on the Flow Control Mechanism of SpaceWire

ZHAO Yun-fu, WU Yi-fan, SUN Qiang, XU Na, WU Jun

(Beijing Institute of Control Engineering, Beijing 100190, China)

Abstract: To solve the problem of SpaceWire performance degradation, which is caused by the current SpaceWire flow control mechanism when SpaceWire interface transfers the bulk data, a Two-Level memory structure is proposed. The current applications and the existing problems about SpaceWire are introduced. By analyzing the flow control mechanism of the SpaceWire and the factors impacting the bus efficiency and the whole system performance, a Two-Level memory structure, which ensures the first level memory have sufficient space to receive or transfer the bulk data, is proposed. Based on SpaceWire protocol and the Two-Level memory structure, a SpaceWire node IP Core is designed, which can effectively control bulk data transfer through hardware prefetching. Finally, while the IP Core is integrated with the LEON3-FT processor, system level simulation and testing are carried out. The results show that, compared with the conventional SpaceWire node, this design can improve 62.7 times in bus efficiency, and at least 14.5 times in system processing data efficiency when it transfers the bulk data.

Key words: SpaceWire; flow control mechanism; bulk data; two-level memory; hardware prefetching

作者简介:

赵云富 男, (1981-), 硕士, 研究方向为 SOC 技术、星载总线技术、大规模集成电路的抗辐射加固技术。

E-mail: zhaoyun6057@163.com