基于数模混合技术的高中频快速AGC电路设计

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摘 要：针对无线通信系统对接收机的高数据传输速率和快速响应速度要求，提出一种基于数模混合技术的高中频快速自动增益控制(AGC)电路的设计方法.该方法首先利用基于FPGA的数字开环结构对后级可调增益放大器进行增益粗调，确保AGC的快速收敛.接着引入模拟闭环结构对可调增益放大器进行增益细调，从而确保AGC输出信号功率的精确稳定.最终利用该方法成功设计实现了一个工作频率305±60 MHz的AGC电路.实验结果表明，该电路具有极高的收敛速度(响应时间小于1μs)，在输出功率稳定在−11.6 dBm的条件下，输入动态范围达到34 dB，并且在120 MHz通带内保持了良好的功率平坦度.该方法为实现高中频快速AGC电路提供了灵活与可重复的设计平台.

关键词：自动增益控制；数模混合技术；收敛速度；高中频；FPGA
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The Design of High Intermediate Frequency Fast Automatic Gain Control Circuit Based on Digital-analog Mixed Technology

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Abstract: This paper proposed a design method of high intermediate frequency (IF) fast automatic gain control (AGC) circuit based on digital-analog mixed technology to satisfy the demands of high data transfer rate and rapid response speed of receivers in modern wireless communication systems. In this method, a digital open-looped structure was adopted for coarse tuning of post-stage variable gain amplifier (VGA) to ensure the fast convergence speed of AGC. Then an analog closed-looped structure was deployed for fine tuning of VGA so as to obtain an accurate and stable output signal of AGC. To validate the proposed method, an AGC circuit with operating frequency of 305±60 MHz was designed and fabricated. Experimental results show that the AGC circuit has an extreme fast convergence speed and its response time is just within 1 μs. The power dynamic range of input signal is 34 dB when a −11.6 dBm output signal is maintained. The power flatness of the circuit is also quite well by the way. The proposed method provides a design platform to implement a high IF fast AGC circuit flexibly and reproducibly.

Key words: AGC; digital-analog mixed technology; convergence speed; high IF; FPGA

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