Flash型FPGA单粒子瞬态脉冲分段滤除电路设计

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摘 要：为提高FPGA在辐射环境条件下的抗单粒子脉冲(SET)的能力，设计了一种由多个延时单元和并联逻辑保护单元(Guard Gate，GG)构成的SET脉冲分段滤除电路. 将SET脉冲处理延时减小至传统方法的10.42%～49.8%，从而提高电路对SET脉冲的处理能力，同时占用的逻辑资源未有明显增加.

关键词：单粒子瞬态脉冲；逻辑保护单元；Flash型FPGA
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Segmented Filtering Circuit for SET Pulse in Flash-based FPGAs

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Abstract: A segmented filtering circuit with delay units and guard gates is proposed to filter SET pulses with different width，considering the range and distribution of SET pulse widths produced in FPGA and the propagation induced pulse broadening. Dividing the widths of SET pulses into several intervals，parallel guard gates with different delay buffers generate corresponding results to different intervals. According to the results，this circuit selects the output in the shortest time，improving the performance on dealing with SET pulses. Simulation results in Fusion family flash-based FPGA indicate that，compared to traditional methods，the segmented filtering circuit can cut the filtering delay of SET pulse in critical path down to 10.42%～49.8%，while power consumption decreasing and no hardware resource increase.

Key words: single event transient；guard gate；flash-based FPGA

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