一种自参考的可变分辨率片上抖动测量系统

解俊杰[1,2],杨雅娟[1,2],刘 飞[1],杨海钢[1],韦援丰[1,2],王 峰[3]
(1 中国科学院 电子学研究所,北京 100190;2 中国科学院大学,北京 100049;
3 龙芯中科技术有限公司,北京 100190)

摘 要:提出了一种基于游标延时链结构的可变分辨率片上时钟抖动测量系统.为消除外部参考时钟引入的误差,利用单周期延时模块实现了自参考抖动测量设计.游标延时链由数字可控延时单元构成,测量分辨率可通过选择信号进行设置.数据读出部分采用真单相时钟D触发器,实现了高速时钟测量.与传统方法相比,此方法无需参考时钟,测量频率范围大,测量分辨率高且可以灵活设置.系统采用0.13 μm CMOS工艺设计,电源电压为1.5 V.后仿结果表明该系统可测量时钟频率范围为100~800 MHz,最高分辨率可达5.71 ps,最大测量量程可达1.4 ns.

关键词:自参考结构;游标延时链;数字可控延时单元;真单相时钟
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A Variable Resolution On-Chip Jitter Measurement System Using Self-Referred Architecture

XIE Jun-jie[1,2], YANG Ya-juan[1,2], LIU Fei[1],
YANG Hai-gang[1], WEI Yuan-feng[1,2], WANG Feng[3]
(1 Institute of Electronics, Chinese Academy of Sciences, Beijing 100190, China;
2 University of the Chinese Academy of Sciences, Beijing 100049, China;
3 Loongson Technology Co., Ltd, Beijing 100190, China)

Abstract: This paper proposes a variable resolution on-chip jitter measurement system which is based on a vernier delay line. In order to eliminate the error introduced by external reference clock, a self-referred architecture is realized by using a one-period delay module. The vernier delay line is composed of digitally controlled delay elements, and the resolution could be set by a selection signal. True single phase clock D flip-flops are adopted in the read-out part to achieve high speed jitter measurement. Compared with traditional methods, the proposed system gains the larger frequency range and the higher measurement resolution, and need not the reference clock. The system is designed in a 0.13 μm CMOS process with 1.5 V supply power. Post-layout simulation results reveal that the system can measure clock jitter various from 100 MHz to 800 MHz with a highest timing resolution of 5.71 ps and a largest range of 1.4 ns.

Key words: self-referred architecture; vernier delay line; digitally controlled delay element; true single phase clock

作者简介:
解俊杰 男,(1990-),硕士研究生.研究方向为大规模集成电路设计.

杨海钢(通讯作者) 男,(1960-),研究员,博士生导师.研究方向为微电子学与集成电路技术、可编程信号处理器架构与Soc设计.E-mail:yanghg@mail.ie.ac.cn.

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