高精度Σ-Δ ADC中多通道数字抽取滤波器的设计

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摘 要：针对传统ADC转换精度较低的缺陷，提出一种24位高精度Σ-Δ ADC的系统设计方法，并完成了数字抽取滤波器的版图设计. 数字抽取滤波器主要由控制模块、7级CIC滤波器、FIR补偿滤波器、FIR抽取滤波器组成. 采用抽取因子可调的多级CIC抽取滤波器结构，有8种输出采样率可供选择，以适应带宽不同的信号. 整体滤波器的通带波纹小于0.05 dB，阻带衰减不低于130 dB. 采用通道间时分复用的方法，相比传统时分复用进一步减少了电路中加法器和乘法器. 采用SMIC 0.18 μm CMOS工艺实现，芯片面积平均每通道约为0.81 mm^2，输出采样率为500 SPS时，平均每通道功耗约为18.26 mW.

关键词：Σ-Δ ADC；多通道；抽取因子可调；较小面积
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Design of Multi-channel Decimation Filter in High Conversion Prescision Σ-Δ ADC

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Abstract: To deal with the low conversion precision of traditional ADC, a design of Σ-Δ ADC with 24-bit high conversion precision was introduced, and digital decimation filter of which was fabricated. The digital decimation filter consists of a controller, a seven stage CIC filter, a FIR compensation filter and a FIR decimation filter. Multi-stage variable decimation CIC filter with 8 output sample rate was proposed to fit different bandwidth signal. Pass band ripple of the combined filters was less than 0.05 dB, and the stop band attenuation was greater than 130 dB. Method of time division multiplexing between different channels was adopted to reduce more adders and multipliers than conventional time division multiplexing. Designed in SMIC's 0.18-μm CMOS process, the chip area was 0.81mm^2 per channel. The circuit consumed only 18.26mW of power per channel when the output sample rate was 500 points per second.

Key words: Σ-Δ ADC; multi-channel; variable decimation; lower area

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