基于脉动阵列的矩阵乘法器硬件加速技术研究

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摘　要:针对卡尔曼滤波算法中矩阵乘法运算的求解问题,比较不同的硬件加速设计方案,利用 9 个自行设计的处理单元,设计了一种基于脉动阵列的并行结构浮点矩阵乘法器,其峰值性能可达 761.96MFLOPS,在资源一定的情形下提高了算法实现的实时性.结合矩阵分块算法,乘法器可对更高维的矩阵进行乘法求解,具有良好的扩展性.

关键词:脉动阵列;矩阵乘法;硬件加速;卡尔曼滤波

Hardware Acceleration Technology of Matrix Multiplier Based on Systolic Array

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Abstract:In KALMAN filtering algorithm,a mass of matrix multiply operation exist. Considering various hardware acceleration technology,based on systolic array,a kind of floating matrix multiplier,with parallel architecture,in order to guarantee the real-time performance,is designed. Nine self-designed PE are integrated in the multiplier,the peak performance of which can reach 761.96 MFLOPS. In the company of Block Matrix Multiplication,the multiplier could be extended well and play a role in higher dimension matrix multiply operation.

Key words:systolic array;matrix multiply;hardware acceleration;KALMAN filtering

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