基于 VHDL-AMS 的流水线 ADC 结构式

建模方法与仿真

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摘 要： 目前很多模数转换器（ADC）缺乏仿真模型，为了大型模数混合信号系统建模与仿真的需要，提出一种基于 VHDL 模拟混合信号扩展（VHDL Analog and Mixed-Signal Extensions，VHDL-AMS）的流水线 ADC 结构式建模方法.以多比特位每级的 12 位分辨率、10 MSPS 流水线 ADC 作为建模对象，根据流水线 ADC 的结构特征，在考虑非理想因素误差情况下，分别建立采样保持放大和乘法数模转换器的 VHDL-AMS 子模型，然后通过例化建立顶层流水线 ADC 的结构模型.通过 SystemVision 和 Simulink 联合仿真，得到静态性能参数微分非线性度和积分非线性度均小于 1 LSB，动态性能参数无杂散动态范围 94.941 7 dB，总谐波失真-94.941 9 dB，信噪比 58.754 4 dB，验证了所提建模方法合的理与有效.

关键词： VHDL-AMS；流水线模数转换器；结构模型；联合仿真

Constructral Modeling Method and Simulation for Pipeline ADC Using VHDL-AMS

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Abstract： A large amount of analog-to-digital converters(ADC) lack of simulation model now, a constructral modeling method for pipeline ADC using VHDL Analog and Mixed-Signal Extensions (VHDL-AMS) is proposed in this paper in order to meet the necessary of modeling and simulation of large analog/mixed signal system. Multi-bit/stage 12 bit, 10 MSPS pipeline ADC is taken as modeling object, accroding to its architectural character, the VHDL-AMS sub-model of Sample-Hold Amplifier and Multiplying Digital to Analog Converter is built respectively with taking account of nonideal factors, and then the architectural model of high level pipeline ADC is built by instantiating. By the co-simulation of SystemVision and Simulink, intatic performance parameter Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are all less than 1 LSB; dynamic performance parameter Spurious Free Dynamic Range (SFDR) is 94.9417 dB, Total Harmonic Distortion (THD) is -94.9419 dB, Signal to Noise Ratio (SNR) is 58.7544 dB. The result shows that the proposed modeling method is reasonable and verified.

Key words： VHDL-AMS; pipeline ADC; constructral model; co-simulation

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