一种 900 V JTE 结构 VDMOS 终端设计

石存明，冯全源，陈晓培

（西南交通大学 微电子研究所，四川 成都 611756）

摘　要：垂直双扩散金属氧化物场效应晶体管（Vertical Double-diffused Metal-Oxide-Semiconductor Field Transistor，VDMOS）是由 Pbody 与外延层之间形成的 PN 结承受电压，由于工艺限制，元胞区域只能设计为突变结，而终端区域最常用的结构为场限环，在原理上也相当于突变结耐压.结合结终端扩展(Junction Termination Extension，JTE)技术，引入缓变结耐压，设计了一款 900 V 的终端结构，实现了 992.0 V 的仿真击穿电压，终端效率达到了 98.6%，而且有效终端长度仅有 130.2 μm，在较大程度上减小了芯片的占用面积，提高了击穿电压，而且工艺流程与成熟的深阱场限环基本一致，有较好的兼容性.

关键词：终端；结终端扩展；缓变结；击穿电压

Design of 900 V JTE Structure VDMOS Termination

SHI Cun-ming, FENG Quan-yuan, CHEN Xiao-pei

(Institute of Microelectronics,Southwest Jiaotong University, Chengdu 611756， China)

Abstract： The breakdown voltage of Vertical Double-diffused Metal-Oxide-Semiconductor Field Transistor(VDMOS) is withstood by the PN junction form by Pbody and EPI. The cell region is designed as a abrupt junction because of the technique limitation.Field Limit Ring(FLR) is the most common structure used in termination region, and it can also take as a abrupt junction. In this paper, a 900 V termination structure is designed with the introduction of graded junction and the combination of Junction Termination Extension(JTE). The simulation breakdown voltage 992.0V with the effective termination length of only 130.2 μm, and the efficiency is 98.6%. The chip area is significantly decreased, breakdown voltage is significantly increased, and the technique is the same to deep well FLR's, which means a good technique compatibility.

Key words： termination； variation of lateral; doping； breakdown voltage

作者简介：

石存明　男，（1989-），硕士研究生.研究方向为大功率器件的研究与设计.E-mail:974743181@qq.com.