基于排序网络的大数逻辑门电路设计

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摘　要： 针对传统大数逻辑门（Majority Logic Gate，MLG）高开销的问题，构造了基于排序网络的 MLG 电路，并以 8 输入的排序网络为例，使用两个 4 输入排序网络、四个与门以及 1 个或门来实现大数逻辑值.采用 VerilogHDL 编写代码，使用 ModelSim 仿真工具进行了功能验证.相比于传统的 MLG，该电路可以有效地缩小 45.11 %的面积、降低 60.43 %的功耗和减小 35.44%的延迟冗余.仿真结果表明，构造的电路可以完成正确的大数逻辑功能.

关键词： 存储器；大数逻辑门；排序网络；单粒子翻转

Design of Majority Logic Gate Circuitry Based on Sorting Networks

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Abstract：The Majority Logic Gate (MLG) has already been used to improve the reliability of memories. As to the issue of high overheads for Majority Logic Gate, a novel MLG circuitry based on Sorting Networks is proposed. An 8-input MLG example, realized in Verilog HDL and simulated by ModelSim, has been shown to explain the structure, which includes two 4-input sorting network, four and-gates and an or-gate.Compared with the traditional MLG circuitry, the proposed circuitry can reduce 45.11% area, 60.43 % power, and 35.44 % delay overheads respectively. The obtained results have shown that the proposed circuitry can achieve Majority Logic function rightly.

Key words：memory; majority logic gate (MLG); sorting networks; single event Upset (SEU)

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