

基于 TDICE 单元的 SRAM 抗 SEU 加固设计

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摘 要: 双立互锁存储单元 (DICE), 在保持状态下是一种可靠有效的单粒子翻转 (SEU) 加固方法, 但是, 基于 DICE 单元的 SRAM 在读操作下会发生抗 SEU 失效. 相比抗单个敏感节点翻转的效果, DICE 抗多个敏感节点翻转的能力较弱. 为此, 在 DICE 结构的基础上采用读写分离机制, 以解决 DICE 单元在读写过程中的节点翻转问题. 同时, 根据电阻加固原理, 在 DICE 存储单元的节点之间增加 NMOS 管, 即 TDICE (Transistor DICE) 结构, 其利用晶体管隔离反馈回路中的节点间的连接, 提高了 SRAM 的抗多节点翻转能力. Spectre 仿真结果表明: 基于 TDICE 单元的 SRAM 具有较强的抗单粒子翻转能力.

关键词: SRAM; 单粒子翻转; DICE; 读写分离; TDICE

Hardened SRAM Design Based on TDICE Cell

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Abstract: Dual Interlocked Storage Cell (DICE) is a reliable and effective method for Single Event Upset (SEU) reinforcement in maintaining state. However, SEU still occur in DICE cell-based SRAM, due to the weakness of DICE cell during reading and writing. Compared with the single node, the effect of DICE resistance multiple-node upset is weak. A separated-read-write structure is proposed to handle the DICE cell's upset during reading and writing. And according to the resistance reinforcement principle, Transistor DICE (TDICE) is used that adding NMOS between the events of DICE. TDICE increases the effect of DICE resistance multiple-node upset through the connection between events in a transistor isolation feedback loop. The simulation results show that, TDICE shows a nearly complete tolerance SET with multiple-node upset. Spectre simulation results show that the SRAM based on the TDICE unit has a strong ability to resist a single event upset.

Key words: SRAM; single event upset; DICE ; separated-read-write structure; TDICE

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