

一种可支持硬件触发机制的灵活可配 PWM IP 核的设计与实现

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摘 要: 提出了一种具有高可配性、高实时性和较强适用性等特点的脉冲宽度调制 IP 核的设计. 该 PWM 模块不仅可支持片上系统内硬件触发反馈机制, 以加强片内 IP 核之间的互联性, 而且还提供了模块内部资源共享的实现方案. 仿真验证的结果表明: 此模块可支持多种输出模式, 且其硬件触发的消耗时间比传统的软件触发的时间少了两倍多. 因此, 该模块可满足可配性高、适用性强和实时性高等设计需求, 达到了设计预期的目的.

关键词: 可配性; 实时性; 适用性; 硬件触发; 资源共享; 仿真验证

Design and Implement of a Configurable PWM IP Core With Hardware Trigger Mechanism

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Abstract: A pulse width modulation (PWM) IP core that having the advantages in configuration, instantaneity and applicability is proposed in this paper. Not only does the PWM IP core support hardware trigger and feedback mechanism for enhancing interconnection among IP cores in the System-on-a-Chip (SoC), but it can also offer a practical scheme with resource reuse inside the PWM IP core. Finally, according to comparative and analytical results of simulation and verification, they indicate that PWM IP core can support multiple output modes, and consuming time of hardware trigger is two times less than traditional software trigger' s by building environment of simulation, editing excitation of test and using tools of simulation. In conclusion, it can meet needs of different configuration, high instantaneity and efficient applicability for achieving design' s aim.

Key words: configuration; instantaneity; applicability; Hrdware trigger; resource reuse; simulation and verification

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