低能耗三输入 AND/XOR 门的设计

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摘　要： 提出了一种基于传输门逻辑的低能耗三输入 AND/XOR 门设计电路.基于 55 nm CMOS 工艺，采用 HSPICE 仿真软件在不同工艺角下对门电路进行后仿真分析，并与已有的 AND/XOR 门电路进行对比.仿真结果表明该电路的性能良好，在典型工艺角下，提出的电路的功耗、速度和功耗-延时积的改进量最高分别可达 10.08%，29.03%与 36.12%，满足低能耗的设计要求.

关键词： 与/异或；功耗；功耗-延时积；低能耗

Design of Low Energy Consumption 3-Input AND/XOR Gate

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Abstract： A transmission gate logic based low energy consumption 3-input AND/XOR gate is proposed. Under 55 nm CMOS process, the post-simulations of the circuit under different process corners are carried out by using HSPICE and compared with the published circuits. The simulation results show that the performance of this circuit is good, under typical process corner, the improvement of the proposed circuit can be up to 10.08%, 29.03% and 36.12% respectively in terms of the power, delay and power delay product, which meets the design requirement of low energy.

Key words： AND/XOR; power; power delay product; low energy consumption

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