基于多核网络处理器的时间感知整形技术研究与实现

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摘 要：时间感知整形（Time Aware Shaper，TAS）是时间敏感网络（Time-Sensitive Network，TSN）的关键机制，对于 TAS 的研究与实现具有重要意义.基于多核网络处理器设计了 TAS 机制功能模块结构和 TAS 引擎处理流程，针对由于内核时钟与 PTP(Precision Time Protocol)时钟存在误差而导致的时隙长度偏差问题，提出了调整保护时隙算法来校正时隙.最后，基于 Cavium 多核网络处理器实现了 TAS 机制，实验结果表明：TAS 机制可以按照预配置时隙发包；增加保护时隙调整，可以有效的校正时隙误差，增加 TAS 机制的鲁棒性.

关键词： 时间敏感网络；TSN；时间感知整形；多核网络处理器

Research and implementation of Time-Aware Shaping mechanism based on multi-core network processor

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Abstract：The Time-Sensitive Networks (TSN) provides important network technology support for “Made in China 2025” plan. The design and implementation of the Time Aware Shaper (TAS), the fundamental mechanism of TSN, is of great significance. In this paper, based on the multi-core network processor, we propose a method for quantifying the bandwidth into time slots and design the function module structure and the processing flow of the TAS mechanism. Moreover, for the problem of time slot length variation caused by the error between the CPU clock and the PTP (Precision Time Protocol) clock, we propose a protection band adjustment algorithm to correct the time slot of the port. Finally, we develop the TAS mechanism based on the Cavium multi-core network processor. The experimental results show that the TAS mechanism can send packets according to the pre-allocated time slots. Besides, enabling the protection band adjustment can effectively correct the time slot error and increase the robustness of the TAS mechanism.

Key words： Time-Sensitive Networks; Time Aware Shaper; multi-core network processor

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