一种基于忆阻器的可扩展乘法器设计

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摘　要：针对在基于忆阻器的全加器设计中，在级联时前级结构需要向后级结构输出的结果以阻值的形式储存在忆阻器中无法直接获取的问题，设计了一种将忆阻器的阻值转换为电压值以方便输出的新结构.基于提出的新结构，改进了基于忆阻器的全加器设计，以此为基础设计了基于忆阻器的乘法器，并实现了乘法器的位宽扩展.以两位乘法器为例，基于 HP 模型，利用 LTspice XVII 仿真，展示提出的读出结构可以有效支持乘法器的位宽扩展.

关键词：忆阻器；全加器；布尔逻辑门；乘法器；扩展

An expandable multiplier design based on memristor

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Abstract：For memristor-based full adder, the output result of pre-structure is necessary to be transferred to the post-structure, which is stored in the form of resistance value and cannot be utilized directly by the post-structure. Targeting at this problem, a novel read-out structure is proposed which converts the value of memristor resistance into voltage value. Based on the proposed structure, a memristor based full adder has been improved and based on this memristor based multiplier is designed and bit-width can be freely expanded. By two-bit multiplier example, based on HP memristor model and by LTspice simulation, it is demonstrated that the proposed structure can efficiently support bit-width expandation of memristor based multiplier.

Key words：memristor; full adder; boolean logic gate; multiplier; extension

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