基于级联结构的低抖动小数分频频率综合器研究

冯向明，曲　明，刘林海

(中国电子科技集团公司 第五十四研究所，河北 石家庄 050081)

摘　要：为了更好的抑制由差分积分调制器（DSM，Delta-sigma modulator）引起的量化噪声、降低小数分频时钟源的时钟抖动，本文提出了一种基于双锁相环级联的抖动消除技术.通过前级整数分频锁相环的倍频提升后级小数分频锁相环 DSM 的工作频率，抑制系统的量化噪声；针对后级参考频率过高，引发相差转化困难的问题，本文提出一种新型的高速电荷泵，在不增加功耗的前提下更好地实现电流的动态匹配.基于 180 nm CMOS 工艺完成级联系统设计，仿真结果显示系统输出频率范围为 3~4 G，抖动为 137 fs，功耗为 47.7 mW.

关键词：低抖动；级联；双环锁相环；量化噪声

Research on Low Jitter Phase-Locked Loops Based on Cascaded Topology

FENG Xiang-ming,QU Ming,LIU Lin-hai

(The 54th Research Institute of China Electronics Technology Group Corporation, Shijiazhuang 050081, China)

Abstract：In order to suppress the quantization noise caused by the Delta-sigma modulator (DSM) and reduce the clock jitter of the fractional-N clock source, a novel jitter reduction technique based on cascaded Phase-Lock Loops (PLL) is proposed. By multiplying the frequency of the first stage to increase the operating frequency of the DSM, the quantization noise is suppressed. Meanwhile, for the difficulties of phase conversion caused by the high-frequency reference, a high-speed charge pump is proposed in this paper, which realizes the dynamic matching of the current without increasing the power consumption. The prototype of the cascaded PLL is implemented on the 180 nm CMOS process and the simulation results show that the output frequency range is 3~4 G, with 137 fs jitter performance and the total power consumption is 47.7mW.

Key words：jitter; cascade; dual-PLL; quantization noise

作者简介：

冯向明　,（1992-),硕士研究生.研究方向为模拟集成电路设计.E-mail:18532101386@163.com.

曲　明　,（1982-）,硕士,高级工程师.研究方向为模拟集成电路设计.

刘林海　,（1971-）,硕士, 高级工程师.研究方向为射频及微波集成电路设计.