一种适用于三维芯片间时钟同步的全数字延时锁定环设计

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摘要： 本文提出了一种适用于三维集成电路芯片间时钟同步的全数字延时锁定环设计.在给定的三维集成电路中，该全数字延时锁定环采用可变逐次逼近寄存器控制器设计来缩短锁定时间，以消除谐波锁定问题并拓宽工作频率范围，实现硅过孔引起的延时偏差可容忍和垂直堆叠芯片间时钟信号同步.整个设计采用 TSMC 65 nm CMOS 低功耗工艺实现.仿真结果显示在工艺角最坏情况下最高工作频率是 833 MHz（SS，125℃，1.08 V），在工艺角最好情况下最低工作频率是 167 MHz（FF，-40℃，1.32 V），整个工作频率范围内最长锁定时间固定为 103 个输入时钟周期，在典型工艺角下功耗为 0.8mW@833 MHz（TT，25℃，1.2 V）.版图有效核心面积为 0.018 mm2.

关键词： 全数字延时锁定环；时钟同步；三维集成电路

Design of ADDLL for 3D-IC Die-to-Die Clock Synchronization

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Abstract： In this paper, an all-digital delay-locked loop (ADDLL) for die-to-die clock synchronization of three-dimensional integrated circuit (3D-IC) is presented. The proposed ADDLL can endure the delay variations between through silicon vias and synchronize the clock signals between vertically stacked dies of the given 3D-IC. In order to solve the harmonic lock problem and widen the operating frequency, the circuit shortened the lock process by the use of variable successive approximation register-controlled scheme. The presented ADDLL is implemented using the TSMC 65 nm CMOS low power technology, and the simulation results show that the highest operating frequency is 833 MHz at the worst case (SS, 125 ℃, 1.08 V), the lowest operating frequency is 167 MHz at the best case (FF, -40 ℃, 1.32 V), the longest lock time is 103 cycles of the input clock, and the power consumption is estimated to be 0.8mW@833MHz at the typical case (TT, 25 ℃, 1.2 V). The area of the ADDLL per die is 0.018 mm2.

Key words： all-digital delay-locked loop; clock synchronization; three-dimensional integrated circuit

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