一种高可靠 SoC 芯片的系统级设计方法

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摘要：为了实现 SoC 在系统级的高可靠设计，文本搭建了一个包括 PowerPC、DRAM、DMA、SRAM 模块的 SoC 系统级设计平台，并采用 VCI 总线协议实现互连.针对高可靠性问题，本文提出并实现了三模冗余与 ECC 纠错编码相结合的存储加固方法，通过一个图像数据处理程序，分析比较了利用冗余和编码带来的可靠性提升.系统级仿真结果表明，本文提出的高可靠设计可以显著提高 SoC 的可靠性.
关键词： 系统级芯片；三模冗余；错误检测和纠正；电子系统级设计；高可靠

A System Design Methodology for High Reliable SoC

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Abstract： In this paper, the reliability problem of the SoC is analyzed in system level. In order to implement the high reliable SoC in system level, a SoC system is designed which includes VCI bus, PowerPC processor, DMA controller, SRAM and DRAM interfaces. As for the high reliable SoC, this paper proposed a high reliable storage mechanism based on a TMR and ECC hybrid structure. An image processing program is design to simulate the reliability of the SoC system in system level. The simulation result shows that the proposed high reliable structure can improve the reliability of the SoC system.
Key words： SoC; TMR; ECC; ESL; high reliability

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