一种低相噪低杂散 1.08GHz 锁相环设计

王征晨，王兴华，武照博
（北京理工大学 信息与电子学院 北京市硅基高速片上系统工程技术研究中心，北京 100081）

摘要： 基于 TSMC90 nm CMOS 工艺设计了一款高性能锁相环.深入分析了电荷泵的噪声和杂散性能，讨论了 LC 压控振荡器的锁定范围理论计算以及相位噪声，并且给出了环路滤波器的设计方法.通过 MATLAB 软件对锁相环整体相位噪声进行系统建模与分析，以优化锁相环的整体相位噪声.整体芯片面积为 530 μm×720 μm，功耗为 33 mW.测试结果表明，在频偏 1 MHz 处的相位噪声为-110.6 dBc，参考杂散-56.935 dBc.
关键词： 锁相环；相位噪声；参考杂散

Design of a Low Phase Noiseand Low Spur 1.08 GHz PLL WANG

Zheng-chen, WANG Xing-hua, WU Zhao-bo
(School of Information and Electronic, Beijing Institute of Technology, Beijing Silicon SoC Engineering Research Center, Beijing 100081, China)

Abstract： A high performance PLL (Phase Locked Loop) is designed and implemented in TSMC 90 nm CMOS Process. The noise and reference spur of the charge pump are analyzed in detail. The theoretical calculation of LC VCO (Voltage Controlled Oscillator) turning range is presented and its phase noise is discussed. The design methods of loop filter is studied. In order to optimize phase noise, the PLL is analyzed by MATLAB. The PLL proposed consumes 33 mW with a 1.2 V power supply and only occupies an area of 530 μm×720 μm. The measured results show that it exhibits an in-band phase noise of -110.6 dBc at 1MHz frequency offset and reference spur is -56.935 dBc.
Key words： phase-locked loop; phase noise; reference spur

作者简介：
王征晨男，(1987-)，博士研究生.研究方向为模拟/射频集成电路设计和测试.E-mail：wangzhengchen1987@163.com.
王兴华女，(1983-)，博士，讲师.研究方向为模拟/射频集成电路设计和测试.
武照博男，(1992-)，硕士研究生.研究方向为模拟/射频集成电路设计.