

# 单路频域窄带抗干扰算法及 FPGA 实现

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**摘要:** 为了降低频域窄带抗干扰算法实现的资源消耗和应用成本, 首先对传统两路的重叠加窗窄带抗干扰算法进行分析, 提出了一种单路频域窄带抗干扰算法. 该算法增加一个数据存取过程, 通过对输入数据的复用, 完成了传统两路的抗干扰处理, 优化了信号处理流程, 减少了算法的计算量. 最后对算法进行了在现场可编程门阵列 (FPGA) 实现, 在实现过程中为了不提高对工作时钟的要求, 设计了专用数据存取模块, 使其能分开输出奇偶两路数据, 并在傅里叶变换 (FFT) 模块中定制了并行蝶形运算单元. 改进的硬件架构不仅能够降低功耗, 而且存储资源消耗只相当于传统两路实现方法一半. 因此本文提出的算法及其实现方法可以在低配置的 FPGA 上实现, 极大的降低了硬件成本.

**关键词:** 频域抗干扰; 重叠处理; 反加窗; 基 4FFT; 蝶形运算单元

## Single Channel Frequency Domain Anti-Jamming Algorithm and FPGA Implementation

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**Abstract:** In order to decrease the resource consumption and practice cost on the implementation of frequency domain anti-jamming algorithm, the principle of traditional two channels frequency domain narrow band interference rejection algorithm are analyzed. The algorithm adds a process of data access. The input data is reused to achieve the traditional two channels interference rejection. This way optimizes signal processing flow and reduce the amount of calculation. Finally, algorithm is established in the field programmable gate array. For the purpose of not raising the requirement of clocking frequency in the implementation, the dedicated data access module is designed to export odd-even data individually and paralleled butterfly operation unit of Fourier transform module is also customized. Improved hardware structure not only can reduce power dissipation but also is a half less than traditional two channels implement method in the storage resource. Therefore, the algorithm and implement method proposed in the paper can realize in the low-configure FPGA and lower the hardware cost immensely.

**Key words:** frequency domain anti-jamming algorithm; overlap operation; inverse windowing; radix-4 FFT; butterfly operation unit

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