一种高频 LC-VCO 相位噪声的分析方法

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摘要：基于 25.2 GHz 整数电荷泵锁相环（CPPLL）的设计需求，采用 TSMC90 nm CMOS 工艺设计了一款中心谐振频率为 25.2 GHz 的低相位噪声 LC 压控振荡器.采用单平衡混频器的工作原理，重点分析并建立了关于尾电流源的相位噪声的数学模型，同时进行了合理优化.经过仿真及测试验证，压控振荡器的谐振频率范围为 22.77~28.5 GHz，相位噪声为-100 dBc/Hz@1 MHz，电路功耗为 15 mA.

关键词： LC 压控振荡器；谐振频率；相位噪声；混频原理

A Phase Noise Analysis Method for High Frequency LC - VCO

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Abstract： Based on the design requirement of the 25.2 GHz integer charge pump phase-locked loop (CPPLL), a low-phase noise LC voltage-controlled oscillator with a center resonant frequency of 25.2 GHz was designed by using the TSMC90 nm CMOS process. Based on the working principle of single-balanced mixer, the mathematical model of phase noise of tail current source was analyzed and established and reasonably optimized. The simulation and measure results indicated that the LC voltage-controlled oscillator had a resonant frequency range of 22.75 ~ 28.5 GHz, whose phase noise was -100 dBc / Hz @ 1 MHz, and the circuit power consumption was15 mA.

Key words： LC voltage-controlled oscillator; resonant frequency; phase noise; frequency mixing theory

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