一种应用于隔离通讯芯片的全数字时钟数据恢复电路

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摘　要： 提出一种应用于隔离通讯芯片的全数字时钟数据恢复电路，该时钟数据恢复电路基于单环结构的锁相环进行设计，包括双模式 bang-bang 鉴频鉴相器，带二进制快速搜索算法和抖动抑制数字滤波器的状态机，以及三级环形数控振荡器等组成部分.电路完全基于 0.18 μmCMOS 工艺库标准单元和硬件描述语言设计，具有锁定速度快、可移植性好、输出抖动小等优点.仿真结果表明该全数字时钟数据恢复电路锁定频率范围为 18～80 MHz，能够在 10 μs 内完成频率捕获，输出峰峰抖动 137.13 ps，RMS 抖动 32.39 ps，1.8 V 供电电压下整体功耗为 1.279 mW@40 MHz.芯片整体版图面积 350 mm×250 mm.

关键词： 时钟数据恢复；隔离通讯；抖动抑制算法

An All-Digital Clock and Data Recovery Circuit for

Isolated Communication Chip

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Abstract： A kind of all-digital clock and data recovery circuit for isolated communication chip is proposed in this paper. The all-digital clock and data recovery circuit is based on the design of a single phase-locked loop structure. It is composed of dual model bang-bang phase and frequency detect, digital machine with binary search and jitter suppressive digital filter, and ladder-shaped ring digital controlled oscillator with three level control word. The circuit is based on standard cell and hardware description language design, with fast locking, low jitter and good portability. Simulation shows that the locking range of this all-digital clock and data recovery is 18~80 MHz，and it finish the frequency locked in 10 μs, the measured peak to peak jitter is about 137.13 ps, RM jitter is 32.39 ps. the circuit consumed the power of 1.279 mW@40 MHz at 1.8 V supply, the layout area is 350 μm×250 μm.

Key words： clock and data recovery, isolated communication, jitter suppressive algorithm

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