引入 IP 核的三维 FPGA 结构研究

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摘　要： 为研究 IP 核的引入对三维 FPGA 芯片性能的影响，提出引入 IP 核同质和粗粒度异质两种三维 FPGA 结构.首先，利用二维 FPGA CAD 开源软件构建基于 IP 核和三维开关盒的三维 FPGA CAD 工具.然后，利用该工具从定性和定量的角度对不同堆叠层数引入 IP 核的同质三维 FPGA 结构进行性能分析.实验发现，随着堆叠层数的增加，关键路径延迟逐渐减小；芯片总面积逐渐增加，单层芯片面积逐渐减小.与引入 IP 核的同质三维 FPGA 结构相比，粗粒度异质三维 FPGA 结构的关键路径延迟更小，表明该结构在减小延时方面的有效性.

关键词： 三维现场可编程门阵列；IP 核；堆叠层数；三维开关盒

Three-dimensional FPGA Architecture Embedded with IP Cores

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Abstract： In order to fathom the effect on three-dimensional FPGA performance after IP cores are integrated, two FPGA structures are introduced in this paper:homogeneous 3D FPGAs with IP cores and coarse-grained heterogeneous ones.In the first place, we developed a new FPGA CAD tool, which is an upgrade version of a 2D FPGA CAD tool, to support FPGAs based on IP cores and 3D switch boxes, then use it to analyze the homogeneous 3D FPGA performance in different layers in terms of quality and quantity. Experiments reveal the fact that with the number of chip layer increases, total chip area will rise, in the other hand, critical path delay and chip area per layer fall accordingly. Compared to the homogeneous 3D structured FPGAs (with IP cores), coarse-grained heterogeneous ones have better critical path delay, which proves such structure has the effectiveness on reducing critical path delay.

Key words： 3D FPGA; IP core; stacked layers; 3D switch box

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