一种基于 40 nm CMOS 工艺 12 位 60 MHz 流水线模数转换器

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摘　要： 采用带采样/保持电路，由 10 级 1.5 位每级级电路和最后一级为 2 位 flash ADC 组成的流水线结构，设计了一种 12 位 60 MHz 高性能流水线模数转换器.在设计中采用栅压自举开关降低非线性，采用带增益自举的折叠式共源共栅输入级和 AB 类输出级的运放，采用动态锁存比较器，同时逐级优化级电路中采样电容以及运放的增益和带宽.在 SMIC 40 nm CMOS 工艺下，当输入信号为 1.875 MHz，采样速率为 60 MHz 时， SNDR 为 68.7 dB， SFDR 为 74.6 dB， ENOB 为 11.12 bit，芯片的核心面积为 0.95 mm2，1.1 V 的电源电压下，消耗的总电流为 56 mA.

关键词： 流水线模数转换器；高性能；采样/保持电路；栅压自举开关； 动态锁存比较器

A 12-Bit 60 MHz Pipeline ADC Based on 40 nm CMOS Process

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Abstract： A 12-bit 60 MHz high-performance pipeline ADC is designed in this paper, which consists of sample/hold circuit, 1.5-bit/stage conversion circuit applied from 1st to 10th and a 2-bit flash ADC of the last stage. In this design a gate-bootstrapping switch was used to reduce nonlinear, an operational amplifier with a gain-boosting folded cascade input stage and a class AB output stage was used, dynamic latch comparator was used too, meanwhile, optimizing the sampling capacitor, the gain and bandwidth of the operational amplifier in the circuit stage by stage. In a SMIC 40 nm CMOS process, when the input signal frequency was 1.875 MHz and the sampling frequency was 60 MHz, the SNDR was 68.7 dB, the SFDR was 74.6 dB, the ENOB was 11.12 bits, the core area of chip was 0.95 mm2, the total dissipation current was 56 mA under the 1.1 V supply voltage.

Key words： pipeline ADC; high-performance; sample/hold circuit; gate-bootstrapping switch; dynamic latch comparator

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