

一种双门限语音端点检测算法的 ASIC 实现

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摘 要: 设计了一种基于短时幅度和过零率双门限判决算法的语音端点检测 ASIC 实现电路, 采用基于异步 FIFO 的动态分帧和 CSD 编码技术大大节省了硬件资源开销, 在 Modelsim 和 FPGA 上分别进行了采集的语音信号的检测验证, 结果表明此算法具有硬件实现简单、资源消耗小、检测正确率高的优点.

关键词: 双门限; 语音端点检测; ASIC; FIFO; CSD; FPGA

A Double Threshold Speech Endpoint Detection

Algorithm Implementation in ASIC

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Abstract: A kind of speech endpoint detection ASIC circuit is designed, which is based on double threshold detection algorithm of short-term magnitude and zero-crossing rate. We can greatly save the cost of hardware resources by using dynamic frame partition technology based on asynchronous FIFO and CSD coding technology. We have completed the verification using the collected speech signal in Modelsim and FPGA platform respectively. The results show that this algorithm has the advantages of simple hardware implementation, low resource consumption and high detection accuracy.

Key words: double threshold; VAD; ASIC; FIFO; CSD; FPGA

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