基于高效约束解决算法的浮点数生成器设计

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摘 要： 为了对微处理器中浮点运算单元 FPU（floating-point unit）进行高效的功能验证，对浮点运算的边界情况进行了研究，引入了对中间结果（intermediate result）的约束解决算法（constriant solved arithmetic）.与传统的对浮点运算单元的功能验证相比，基于该约束算法的浮点数生成器，拓宽了浮点边界情况的可选范围，有效提高了验证效率.实验结果表明，集成该浮点数生成器的 UVM 验证平台，能够在 12 小时的测试时间内，对一个浮点运算子模块（floating-point subunit）达到超过 99%的覆盖率.

关键词： 浮点运算单元；中间结果（IR）；约束解决算法（CSA）

Design of Floating Point Number Generator Based on High-Efficiency Constraint Solving Algorithm

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Abstract： In order to verify the function of the floating-point unit in the microprocessor high-efficiently, numerous corner cases of floating-point arithmetic has been studied. Several arithmetics are introduced to solve the constriants of the intermediate results. Compared with the traditional function verification of floating-point unit, the floating-point number generator based on the constraint solved algorithms has widened the scope of the optional floating-point corner cases, which effectively improves the verification efficiency.Experimental results show that the UVM verification platform which integrated the generator can test one floating-point subunit efficiently,which achieves high coverage beyond 98%,within 12 hours of testing time.

Key words： floating-point unit;intermediate result(IR); constraint solved algorithm(CSA)

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