基于时间域误差反馈滤波器的二阶ΔΣ TDC

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摘 要：在这篇文章中，一个二阶ΔΣ时间数字转换器被提出以获得高的分辨率和宽的信号带宽.所提出的时间数字转换器采用了基于时间域运算电路如时间寄存器、时间加法器等构成的时间域误差反馈滤波器的单环结构.采用 SMIC 28 nm 工艺设计，Spectre 仿真结果表明噪声底约为-84 dBps2/Hz，等效到 50 Msps 没有噪声整形的 TDC 的分辨率约为 1.5 ps，功耗取决于输入时间间隔，在测量间隔 1 ns 时功耗约为 1.24 mW，测量范围可达 7.5 ns.

关键词：时间数字转换器；误差反馈滤波器；噪声整形；时间域

A Second-Order ΔΣ TDC Using Time-Domain Error-Feedback Filter

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Abstract： In this paper, a second order ΔΣ Time-to-Digital Converter (TDC) is proposed to achieve high resolution and wide signal bandwidth. The proposed TDC is a single-loop architecture based on a time-domain error-feedback filter using time-domain arithmetic circuits such as time registers , time adders and so on. Implemented in SMIC 28 nm CMOS process, spectre simulation results shows the noise floor of the TDC by taking the minimum PSD value of 84 dBps2/Hz which corresponds to a 50Msps classical quantizer without noise shaping and with 1.5 ps steps. The TDC power consumption depends on the time difference between input edges, typically about 1.24 mW for 1ns interval measurement, the measurement range can be up to 7.5 ns.

Key words： time-to-digital converter (TDC); error-feedback filter; noise shaping; time-domain

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