浮点及整数混合运算器的设计与实现

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摘 要：针对现行普遍的浮点运算器耗费面积较大，功能实现结构松散的问题，设计实现一款浮点及整数混合运算器(Mixture-Arithmetic Logic Unit， M-ALU).该运算器基于基 4 算法华莱士树型结构，并尝试一种新的阶码对齐方法，合并整数运算与浮点运算处理逻辑.在三级流水线结构下可准确完成单精度浮点数，扩展精度浮点数以及整数基本运算.采用基于 synopsys 提供的 Design Compler 综合工具在 SMIC 65 nm 工艺库下完成综合，达到 500 MHz 主频.

关键词：IEEE754；Systemverilog；乘加运算；整数；浮点

Design and Implementation for a Integer-Float ALU

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Abstract： For solve the issue that commont floating pointe ALU comsumes large area and srtucture loosely,a floating point and integer mixed operator M-ALU are designed and implemented. The algorithm based on the base-4 algorithm Wallace tree structure, and try a new order code alignment method,merging integer arithmetic and floating point arithmetic processing logic. In the three-stage pipeline structure can be accurately completed single-precision floating-point, extended precision floating-point and integer basic operations. Based on the synopsys provided by the Design Compiler synthesis tool in the SMIC 65nm process library to complete the synthesis, to 500 MHz frequency.

Key words： IEEE754；systemverilog；multiply-add operations；interger；floating point

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