变维度 FFT 硬件加速器结构设计及 FPGA 实现

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摘　要：本文设计了一种变维度 FFT 硬件加速器，其采用体-面-线的数据组织形式，提出了一种面划分兼多路并行的架构，从面和线 2 个层次展开计算，以面为基本存储单位，以线为基本计算单位，提高了 FFT 运算的并行度，减少了处理器间的数据交互，并通过乒乓预读取的设计和无冲突的地址调整，提高了整机的运算访存比.本文设计的 FFT 加速器内含 32 个并行计算单元，支持 IEEE-754 标准下的 32 位单精度浮点数 32 点到 64 K 点一维 FFT 运算，32 点到 256 点的二维/三维 FFT 运算，且具有较强的可扩展性，可根据需要实　现 m×n×p 序列的 FFT 运算.该设计已在 Xilinx Virtex6 FPGA 芯片上进行原型验证，最高工作频率 184.88 MHz.

关键词：FFT 硬件加速器；FFT 处理器；地址调整模块；FPGA

Structure Design and FPGA Implementation of a Variable Dimension FFT Hardware Accelerator

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Abstract：In this paper, a variable dimension FFT hardware accelerator is designed. By using the data form of body-surface-line, the calculation is carried out from two levels of surface and line. It adopts surface partitioning and multiple parallel architecture to improve the parallelism of FFT. Furthermore by using Ping-Pong operation, pre-read and flexible address adjustment to conceal data transmitting time. In this paper, the FFT accelerator consists of 32 parallel computing units to carry out 2^n (n is from range of 5 to 16) single-precision floating-point 1-D FFT and 2^n (n is from range of 5 to 8) single-precision floating-point 2-D/3-D FFT. What is more, it is important that the structure has strong expansibility which can achieve FFT of the sequence of m×n×p. As a result the design's maximal frequency is up to 184.88 MHz. It has been successfully applied on the Xilinx Virtex6 FPGA chip.

Key words：FFT hardware accelerator; FFT processor; the module of address adjustment; FPGA

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