FPGA 板级自动化仿真测试环境框架设计

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摘　要：针对当前 FPGA 测试过程中，板级测试存在的实施代价高、测试充分性受限、测试可信度差等问题，提出了一种自动的、实时的、非侵入性的闭环半实物仿真测试环境，通过真实的物理接口测试技术、动态总线数据技术和外部对象仿真建模技术，将目标 FPGA 运行环境映射至板级自动化仿真测试环境，并对测试环境进行任务结构、物理结构的定义和划分，围绕测试数据的产生消费过程设计测试环境的工作过程，最后基于该框架开发了测试工具的基本原型，并在测试项目中取得了较好的效果.

关键词：FPGA；板级测试；自动化测试；仿真测试；测试环境

Framework Design of Automatic Simulation Testing

Environment for FPGA Board Level Test

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Abstract：There are many problems in the current process of FPGA testing, such as high cost of implementation, limited sufficiency of testing, and poor reliability of result. An automatic, real-time, non intrusive and closed loop simulation test environment is presented. In the design of the environment, it maps the target FPGA environment to the board level simulation test environment through the physical interface technology, the dynamic data technology and the external device simulation technology. The framework of the environment, the task structure and physical structure for the test environment is defined, the working process based on the generation and consumption of test data is designed. Finally, a preliminary prototype based on the framework is designed, which achieves good results in a test project.

Key words：FPGA; board level test; automatic test; simulation test; test environment

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