

可重构视频阵列处理器中全局控制器的设计与实现

张雪婷, 蒋 林, 邓军勇, 吕 青, 武 鑫

(西安邮电大学 电子工程学院, 陕西 西安 710121)

摘 要: 提出了一种基于可重构阵列处理器的视频编解码方案, 重点描述面向算法切换与资源调整的全局控制器设计方法, 通过层次化编程网络将阵列处理器与主机接口相连, 从而实现对视频阵列处理器计算资源的控制与管理. 实验结果表明, 该全局控制器支持多种模式的指令加载以及计算数据的反馈, 在现场可编程门阵列(Field Programmable Gate Array, FPGA)上最高工作频率可达 539.96 MHz, 相较于同类型阵列结构, 全局控制器的执行周期降低了 50%.

关键词: 可重构; 视频阵列处理器; 全局控制器; 层次化编程网络

The Design and Implementation of Global Controller in Reconfigurable Video Array Processor

ZHANG Xue-ting, JIANG Lin, DENG Jun-yong, LV Qing, WU Xin

(School of Electronic Engineering, Xi'an University of Posts and Telecommunications, Xi'an 710121, China)

Abstract: A video codec scheme based on reconfigurable array processor has been proposed. The design method of global controller for algorithms switching and resources adjustment is mainly described. In this design, array processors and host interface has been connected through hierarchical programming network to realize the control and management of computed resources for the video array processors. The experimental results shows that this global controller support various of modes to load instructions and feedback the calculated data. The maximum operating frequency in the field programmable gate array (FPGA) can up to 539.96MHz and compared with the same type array structure, the execution cycle of global controller is reduced by 50%.

Key words: reconfigurable; video array processor; global controller; hierarchical programming network

作者简介:

张雪婷 女, (1993-), 硕士研究生. 研究方向为集成电路系统设计. E-mail: 1014007517@qq.com.

蒋 林 男, (1970-), 教授. 研究方向为专用集成电路设计.

邓军勇 男, (1981-), 博士, 副教授. 研究方向为专用集成电路设计.

吕 青 女, (1989-), 硕士研究生. 研究方向为集成电路系统设计.

武 鑫 女, (1992-), 硕士研究生. 研究方向为集成电路系统设计.