

一款增益可调的 28 nm 三通道 10 位 DAC

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摘要: 基于 SMIC 28 nm CMOS 工艺, 实现了一款增益可调的三通道的 300 MS/s 10 bit 的数模转换器. 此数模转换器可以通过 5 位的控制字实现 0 ~ -5.75 dB 的增益调节, 适应更多的应用环境. 数模转换器采用分段式结构, 其中高六位采用温度计码, 低四位采用二进制码. 在电流源单元开关部分采用限幅电路, 提高无杂散动态范围. 带隙基准单元采用低电压输出结构, 满足电压电流转换单元中的栅压要求. 在 1.8 V 模拟电源电压, 1.05 V 数字电压下, 采样时钟在 300 MHz 的时候, 无杂散动态范围 (SFDR) 为 64 dB, 微分非线性小于 (DNL) ± 0.3 LSB; 积分非线性小于 (INL) ± 0.4 LSB.

关键词: DAC; 数模转换器; 电流舵; 增益控制

A 10-bit 300 MSPS DAC With Variable Gain Based on 28nm Process

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Abstract: This paper presents a variable gain three-channel 10-bit current steering CMOS digital-to-analog converter (DAC) implemented in a standard 28-nm CMOS technology. The DAC achieved variable gain of 0~-5.75 dB with five-bits control words to apply to a wider range of applications. The DAC is segmented as 6+4, where the 4-LSB bits are implemented in binary and the 6-MSB bits are implemented in unary architecture. The spurious free dynamic range (SFDR) of this DAC can be improved by using clipper circuit in the part of switches. The reference voltage of bandgap must be low enough to meet the requirements of bias voltage in the part of voltage changing to current. The circuit is fabricated in 1.8-V analog power supply and 1.05-V digital power supply. For sampling frequencies up to 300MSample/s, the SFDR is better than 64 dB. The measured differential nonlinearity and integral nonlinearity are 0.3 least significant bit (LSB) and 0.4 LSB, respectively.

Key words: DAC; digital-analog conversion; current steering DAC; variable gain

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