

# 一种 Vcm-Based 10 位 16M 采样率低功耗逐次逼近型模数转换器

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**摘要:** 针对无线传感网络中低功耗无线传感器的应用, 设计了一种采样速率为 16 MSPS, 精度 10 bit 的全差分超低功耗逐次逼近型模数转换器 (SAR ADC). 提出一种基于 Vcm-Based 参考电压的开关切换逻辑, 减少 DAC 模块参考电压开关切换的功耗. 同时, DAC 电容阵列模块采用分段式结构, 单位电容采用优化的 MOM 电容, 有效提高 ADC 的匹配性和精度; 此外采用了双尾电流型动态锁存比较器, 实现功耗的最优化. 芯片采用 CMOS 65 nm 工艺设计, 后仿结果显示在 1.2 V 电源电压及 16 MSPS 采样率下, ADC 有效位数达到 9.42 bit, 功耗为 140  $\mu$ W, 品质因数 (FOM) 为 12.8 fJ/Conversion-step.

**关键词:** 逐次逼近型模数转换器; Vcm-Based; 动态比较器; 超低功耗

## A 10-bit 2 Ms/S SAR ADC with Vcm-Based Switching Scheme

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**Abstract:** Aiming at the application of low power wireless sensor in wireless sensor network, a ultra low power Successive Approximation Register Analog-to-Digital Converter (SAR ADC) has been designed. A switching logic based on Vcm-Based reference voltage is proposed to reduce the power consumption of the DAC when the reference voltage is switched. The DAC capacitor array module uses the sectional structure, the unit capacitance uses the optimized MOM capacitance, enhances the ADC matching and the precision effectively. In addition, a double tail current dynamic latch comparator is used to optimize the power consumption. The ADC is implemented in CMOS 65 nm technology. The post simulation results shown that under 1.2 V supply voltage, the sampling rate is 16 MSPS, the power consumption is 140  $\mu$ W, effective number of bits reached 9.42 bit, and the figure-of-merit (FOM) is 12.8 fJ/conversion-step.

**Key words:** SAR ADC; Vcm-Based; dynamic comparator; ultra low power

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