一种高性能无片外电容型 LDO 设计

程　立，黄　鲁

（中国科学技术大学 电子科学与技术系，安徽 合肥 230027）

摘　要：设计了一种高性能无片外电容型 LDO 线性稳压器.其中，EA 采用推挽输出放大器设计，在静态时保持低功耗，瞬态响应时提供大的输出电流，提高 LDO 的响应速率.高环路增益使 LDO 电路具有很高的稳压精度；采用零点补偿技术，保证了 LDO 环路稳定性.LDO 采用 0.13 μm CMOS 工艺设计，仿真结果表明，在 1.2 V~2.0 V 输入电压下，LDO 输出稳定的 1.0 V 电压，输出负载电流为 50 μA~100 mA，最大负载电容可达到 100 pF，低频 PSR 为 -67.5dB@100mA ~-85.5dB@50μA，负载调整率 0.8μV/mA，LDO 的静态电流为 50 μA，整体版图面积为 0.016 3 mm^2.

关键词：LDO；线性稳压器；无片外电容；电源抑制；高性能

Design of a High Performance Output-Capacitorless LDO

CHENG Li，HUANG Lu

（Department of Electronic Science and Technology , University of Science and Technology of China,

Hefei 230027, China）

Abstract：A High Performance Output-Capacitorless LDO is presented in this paper. In this design, EA applies a push-pull output amplifier, so that it can maintain low power consumption in quiescent state，and provide large output current in the transient response, which greatly improve the response rate. High loop gain allows the LDO circuit to achieve very high regulation accuracy; and using zero compensation technology to enhance the stability of the LDO loop. The LDO is designed in 0.13 μm CMOS process. Simulation results show that the output voltage can be stable at 1.0 V when its supply is range from 1.2 V to 2.0 V. The output load current is from 50uA to 100 mA, the maximum load capacitance is up to 100 pF, PSR at low frequency is -67.5dB@100mA ~-85.5dB@50μA. Load regulation is 0.8μV/mA. The LDO only consumes 50 μA quiescent current, and the overall layout area is 0.0163mm^2.

Key words：LDO; linear regulator; output-capacitorless; PSR; high performance

作者简介：

程　立　男，（1991-），硕士研究生.研究方向为模拟集成电路设计.

黄　鲁(通讯作者)　男，（1961-），副教授，硕士生导师.研究方向为数模混合信号 IC 设计.

E-mail：luhuang@ustc.edu.cn.