

6.25 Gb/s 串行数据接收器设计

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摘要: 设计一款基于 65 nm CMOS 工艺、数据传输速率在 6.25 Gb/s 的 SerDes 接收器, 其中均衡电路采用连续时间线性均衡器; 采样电路采用了一种新型灵敏放大器, 较传统结构将灵敏度提升了一个量级, 同时解决了传统结构输出信号下降沿比上升沿慢一个门延迟的问题; 时钟数据恢复电路 (CDR) 采用半速率采样二阶 CDR 系统实现. 通过仿真验证, 该接收器具有正确逻辑功能, 功耗为 10.2 mW.

关键词: 高速串行; 接收器; 灵敏放大器

Design of 6.25 Gb/s SerDes Receiver

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Abstract: In this paper, a 65 nm CMOS 6.25 Gb/s SerDes receiver is designed. Equalization is achieved by using continuous-time linear equalizer. The sampler employs a novel sense amplifier (SA), which improves the sensitivity by the conventional SA of magnitude and simultaneously solves the problem that falling edge lags rising edge the time of a gate delay; a half-rate second order clock and data recovery system is presented. Simulation results show that the receiver has the correct logic function, the power consumption is 10.2 mW.

Key words: high speed serial link; receiver; sense amplifier

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