一种专用可重构流水信号处理器的设计

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摘　要：可重构流水信号处理器(Reconfigurable Pipeline Signal Processing Core,RPSC)可以通过层次化可配置流水架构实现多种应用，通过粗粒度的静态配置方式，改变 RPSC 中基本流水级的拓扑结构和互连关系，以资源复用的方式实现特定应用的硬件加速，满足信号处理算法对性能以及灵活度的要求.本文针对信号处理算法设计的专用 RPSC 可配置实现信号处理中的两种常用算法：测频算法和阵列信号处理算法，算法中涉及的相应参数也能进行配置，使用方便，各算法间可复用运算资源和存储资源，采用并行和流水的架构实现，满足了灵活性、实时性和数据吞吐率的要求.同时基于 Xilinx Virtex-7 VC707 开发板进行了验证工作，RPSC 的主频为 150 MHz，计算资源的复用率达 47.8%，存储资源复用率达 17.6%，测频算法的吞吐量为 7.2 Gb/s，阵列信号处理算法的吞吐量为 14.4 Gb/s，满足应用需求，验证了该方法的有效性.在实际应用中，还可以通过分析和选取所需实现算法的种类和复杂度，提升主频、资源复用率、灵活度等各方面性能.

关键词：可重构流水信号处理器；并行和流水；资源复用；灵活度

One Design of Specified Reconfigurable Pipeline Signal Processing Core

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Abstract：Reconfigurable Pipeline Signal Processing Core (RPSC) improves the performance and flexibility of various applications by hierarchical reconfigurable architecture. The topology and interconnection of RPSC's basic pipelines are changed by coarse-grained static configuration method. The RPSC specified to signal processing algorithm can be configured to implement two applications: frequency measurement algorithm and array signal processing algorithm. Moreover, it is convenient and flexible to configure the parameters in two different algorithms, in which the resources are reused. Two algorithms implemented use parallel and pipeline architecture to meet the demands of flexibility, real-time and data throughput rate. Based on Xilinx Virtex-7 FPGA VC707 Evaluation Kit, the design is verified with frequency of 150 MHz. The reuse ratios of computing source and memory resource are 47.8% and 17.6%, respectively. The throughputs of frequency measurement algorithm and array signal processing algorithm are 7.2 Gb/s and 14.4 Gb/s respectively and they are enough to meet the requirement for applications. In the practical situation, it is possible to analyze and select suitable applications of different classes and complexity to improve the frequency, reuse ratio and flexibility.

Key words：reconfigurable pipeline signal processing core; parallel and pipeline; resource reuse; flexibility

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