基于 UVM 的浮点功能部件验证

吴升光 1，2，羊箭锋 1，冯春阳 2
（1 苏州大学 电子信息学院，江苏 苏州 215000;2 中晟宏芯有限公司，江苏 苏州 215000）
摘 要：为了对复杂浮点运算单元进行功能验证，设计并实现了一种基于 UVM（Universal Verification Methodology）方法的验证平台.该平台集成了一套高效的浮点数产生机制，将浮点用例的求解转化为连分式的求解，拓宽了传统浮点用例的边界定义，同时也调用了基于 C 语言的参考模型来自检计算结果，并结合 FCC(Fast Coverage Convergence)技术，加快了覆盖率收敛.应用结果表明，此验证平台能够对浮点运算单元各功能进行高效验证，极大地减少验证时间，且平台内嵌的浮点数产生器也能够移植到其他浮点功能验证平台.
关键词：浮点运算单元；UVM 验证平台；中间结果约束；浮点数生成

Verification of Floating Point Facilities Based on UVM

WU Sheng-guang 1，2 , YANG Jian-feng 1, FENG Chun-yang 2
(1 School of Electronic and Information Engineering, Soochow University,Suzhou 215000, China;
2 SPT Co. Ltd. Suzhou 215000,China)
Abstract：A test-bench was designed and implemented on the basis of UVM to verify all facilities of the floating-point unit. The test-bench integrates an efficient mechanism to generate floating-point operands and expands the corner of traditional cases with the method of convert floating point numbers to continued fractions. It calls a C model to achieve automatic results comparison, in addition to FCC technique, the coverage was converged quickly. Experimental results show that the test-bench can effectively verify all facilities of the floating-point unit and greatly reduce the time, moreover, the floating-point generator can be used for other floating-point verification.
Key words：floating-point unit; UVM test-bench; intermediate result constraint；floating-point operand generation

作者简介：
吴升光 男，（1991-），硕士研究生.研究方向为集成电路设计与验证.
羊箭锋（通讯作者） 男，（1978-），副研究员，硕士生导师.研究方向为信号与信息处理.E-mail：jfyang@suda.edu.cn.