一种基于 40 nm CMOS 工艺的电流舵 DAC IP 核设计

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摘　要：基于 SMIC 40 nm CMOS 工艺，设计了一种 10 位 100 MS/s DAC IP 核.该 DAC IP 核采用 6+4 分段式电流舵结构，1.1 V/2.5 V 双电源供电，满量程输出电流为 20 mA.完成了 DAC IP 核电路和版图的原型设计，提取了物理模型与时序模型，组成基本的数据交付项.对该 DAC IP 核进行了仿真分析，给出了流片后的测试结果.

关键词：数模转换器；分段式电流舵；IP 核

Design of a Current-Steering DAC IP Core

Based on 40 nm CMOS Process

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Abstract：Based on SMIC 40 nm CMOS process, a 10 bit 100MS/s DAC IP core was designed. A 6+4 segmented current-steering architecture was employed in the DAC IP core, and the full-scale output current was 20 mA with 1.1 V/2.5 V dual power supplies. For the DAC IP core, the prototype design of circuit and layout was completed, and the physical model and timing model were obtained to form the data deliveries. The simulation analysis of the DAC IP core was carried out, and the test results after tape-out were presented.

Key words：DAC；segmented current-steering；IP core

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