ARM 并行阵列机中的路由器设计

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摘 要：针对 ARM 并行阵列机结构，提出了与之相适应的通信结构，采用 4 个路由器完成 16 个处理器内核之间的通信，有效地节约了面积.该路由器采用基于数据包交换的片上网络通信方式，内部运用缓存机制、经典的 XY 路由算法和专用的仲裁策略再加入数据多播，且处理器选用低功耗、高性能的 ARM 内核，通过采用以上机制能够有效降低数据传播延迟和功耗.实验结果表明采用该方案设计的路由器时钟频率最高可达 406.009 MHz，能够满足该 ARM 阵列机对于通信速率的要求.

关键词：路由器；缓存机制；经典 XY 路由算法；核间通信；数据多播

Router Design for a ARM Parallel Processor

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Abstract：Routing communication structure designed in this paper’s project involves calls ARM parallel array processors that use four routers to complete the communication between the 16-core processors. Therefore it makes the area reduced at a greater degree. The router uses the way of Noc (Network on Chip) communication that is based on the packet switching , it uses internal caching mechanism, classic XY router algorithms, dedicated arbitration policy and data multicast,and with low power of high-performance ARM processor, these mechanisms reduce the data propagation delay and power consumption at the same time. Makes the performance of communication between multi-core processors has been increased greatly. The result shows that the clock frequency of the router, which designs for the telecommunications in the array of ARM muti-core machine, is up to 406.009MHz and the router can better meet the performance requirements of the array of ARM muti-core machine.

Key words：router; caching mechanism;classic XY router algorithms; communication between multi-core processors;data multicast

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