应用于 14 bit 低功耗流水线 ADC 的 sub-ADC 电路设计

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摘　要：基于 SMIC 0.18 μm 标准 CMOS 工艺，设计了一种应用于 14 bit、100 MHz 采样频率低功耗流水线 ADC 的 1.5 位 sub-ADC 单元电路.sub-ADC 主要包括核心模块比较器电路和编码单元电路.采用由前置放大器和锁存器构成的动态锁存比较器，来实现较高的速率.为降低流水线 ADC 的每一级功耗，提出一种新结构的 sub-ADC 电路，实现前置放大器在相邻的比较器中共享，增加复位开关电路降低“回踢”噪声和消除两锁存器之间的相互干扰.仿真结果表明：在 3 V 电源电压、100 MHz 的采样频率下，输入输出正确翻转，传输延时为 1.73 ns，功耗为 157.3 μA，可满足高精度低功耗流水线 ADC 的性能要求.

关键词：流水线 ADC；低功耗；sub-ADC；动态锁存比较器；前置放大器共享

Design of Sub-ADC Applied to 14 Bit Low-Power Pipeline ADC

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Abstract：Design of the 1.5 bit sub-ADC applied to 14 bit low-power pipeline ADC circuit. The circuit is fabricated in a 0.18 μm standard CMOS process provided by SMIC. The sub-ADC mainly includes the core module comparator circuit and the encoder circuit. The high speed is realized by using the dynamic latch comparator which is composed of the preamplifier and the latch. In order to reduce the power consumption of pipelined ADC, a new structure of sub-ADC circuit is proposed, which can realize the sharing of the preamplifier in the adjacent comparator. Increase the reset switch circuit to reduce Kickback noise and eliminate the mutual interference between the two latches. The simulation results show that the input and output correct flip in 100 MHz sampling frequency at 3V supply voltage. The transmission delay is 1.73 ns, and the power consumption is 157.28 uA. Can meet the high accuracy and low power pipeline ADC performance requirements.

Key words：pipeline ADC；low-power；sub-ADC；dynamic latch comparator；low-power；Preamp shared EEACC: 2570

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