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一种改进的 CSA 低功耗阵列乘法器的实现

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摘　要：以实现电能采集中所需求的低功耗、小面积的乘法器为目标，设计了一种 16×16 位高性能阵列改进乘法器.系统采用 Booth-4 编码器产生部分乘积项，通过对部分积重组后并采用改进的 CSA 阵列完成压缩，直接得出乘法结果.这消除了传统并行乘法器的进位加法器部分，节省了大量的晶体管，从而有效降低了系统的整体功耗.设计采用 0.6 μm SMIC 工艺布线，利用 H-spice 工具仿真验证，结果表明当工作在 2.0 V 单输入电压，150 MHz 输入频率时，乘法器系统功耗为 8.98 mW，延迟为 8.76 ns.

关键词：乘法器；低功耗；改进的 CSA 阵列；关键路径；Booth-4 算法

A Low Power Multiplier with Modified Carry Save Array

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Abstract： The low power and small area of the multiplier is widely in the electrical energy acquisition ,A High quality of 16×16 multiplier with Carry Save Array is designed. The modified Booth-4 algorithm is adopted to generate partial product and the design of modified CSA is introduced to compress the partial product, eliminating the propagate adder at the final stage of the conventional multipliers. Due to removal of a few transistors in the array architecture, the proposed multiplier with Carry Save Array reduces the power dissipation and the area. In the design, At the voltage of 2.0 V, the H-spice is used to carry out the results for 0.6μm SMIC technology which reveals the proposed design has a measured power dissipation of 8.98 mW and that multiplication time of multiplier is 8.76ns at a frequency of 150 MHz.

Key words： multiplier; low power consumption; critical path; dual logic; booth-4 algorithm

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